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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,758	10/04/2004	Toshiharu Furukawa	BUR920040090US1	5757
	7590 08/04/200 & BERNSTEIN, P.L.0	EXAMINER		
1950 ROLAND	CLARK DRIVE	DAHIMENE, MAHMOUD		
RESTON, VA 2	20191		ART UNIT	PAPER NUMBER
			1792	
			NOTIFICATION DATE	DELIVERY MODE
			08/04/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

gbpatent@gbpatent.com pto@gbpatent.com

		Applic	ation No.	Applicant(s)		
Office Action Summary		10/71	1,758	FURUKAWA ET AL.		
		Exami	ner	Art Unit		
		****	OUD DAHIMENE	1792		
The MAIL Period for Reply	ING DATE of this commu	nication appears on	the cover sheet with	the correspondence a	ddress	
WHICHEVER IS - Extensions of time m after SIX (6) MONTH- - If NO period for reply - Failure to reply within Any reply received by	STATUTORY PERIOD F LONGER, FROM THE May be available under the provision S from the mailing date of this com is specified above, the maximum so the set or extended period for reply the Office later than three months djustment. See 37 CFR 1.704(b).	MAILING DATE OF s of 37 CFR 1.136(a). In n- munication. tatutory period will apply ar y will, by statute, cause the	THIS COMMUNICA be event, however, may a rep and will expire SIX (6) MONTH application to become ABAI	ATION. ly be timely filed HS from the mailing date of this of NDONED (35 U.S.C. § 133).		
Status						
2a)⊠ This action 3)□ Since this	e to communication(s) file is FINAL. application is in condition ccordance with the pract	2b)∏ This action in for allowance exc	- s non-final. ept for formal matter	· ·	e merits is	
Disposition of Clair	ns					
4a) Of the a 5) ☐ Claim(s) _ 6) ☑ Claim(s) 1 7) ☐ Claim(s) _ 8) ☐ Claim(s) _	-14 and 21-26 is/are pendabove claim(s) is/a is/are allowed. -14 and 21-26 is/are rejection is/are objected to. are subject to restri	are withdrawn from	consideration.			
Application Papers						
10)☐ The drawin Applicant m Replaceme	cation is objected to by the g(s) filed on is/are ay not request that any object drawing sheet(s) including declaration is objected to	: a) ☐ accepted on ection to the drawing(g the correction is red	s) be held in abeyance quired if the drawing(s	e. See 37 CFR 1.85(a).) is objected to. See 37 C		
Priority under 35 U	S.C. § 119					
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 						
	son's Patent Drawing Review (ure Statement(s) (PTO/SB/08)	PTO-948)	Paper No(s)/	mmary (PTO-413) Mail Date ormal Patent Application		

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DETAILED ACTION

Claim Rejections - 35 USC § 103

- 1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).
- 3. Claims 1-8, 11-14, and 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gruner et al. (US 4,538,748) in view of Applicants' Admitted Prior Art.
- 4. Regarding claims 1, 8, 11-14, 21-22, Gruner discloses a thin film circuit wherein the following steps are disclosed: protecting a pair of critical edges of a hard mask (5) (column 4, line 21) on a substrate with a first portion of a second mask (90) (figure 2d) which is considered here as a "follow-on mask" since layer (90) is deposited directly on or following layer (5); forming a wide-image mask on the left and right regions (M1 and

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M3) (as designated in figure 2n) of the substrate proximate the hard mask with a second portion of the second mask (90), here the term wide-image mask is interpreted by the examiner in it's broader sense including "a wide-area mask, is employed to add shapes of any other, usually wider, dimensions"; removing an exposed portion of the hard mask (5); and exposing the pair of critical edges of the hard mask (figure 2i). The edges of Gruner's mask (5) must be critical since they are part of the electrical circuit. In Gruner's method, the second portion (M1 and M3) of mask (90) substantially aligns with a corresponding portion of a final shape.

It is noted that Gruner is silent about an (SIT) loop.

In the "Background Description" section on applicants' specification, applicants' disclose "SIT methods produce structures, usually hard masks, of generally closed-loop geometry. These loops have a single, well-controlled width (referred to henceforth as the "critical image width"). Conventional SIT applications thus require the use of two additional masks. One, called a "loop cutter mask", is employed to segment the loops, and a second, called a wide-area mask, is employed to add shapes of any other, usually wider, dimensions" [Para 5].

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the process of Gruner to any substrate including a substrate comprising a STI loop.

One of ordinary skill in the art would have been motivated to apply the process of Gruner to any substrate including a substrate comprising a STI loop in order to

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effectively protect the edges of layers that are susceptible to damage during the subsequent processing steps as suggested by Gruner.

As to claim 2, in Gruner's figure 2h portions of the exposed hardmask (5) are removed.

As to claim 3, in Gruner's figure 2i the critical edges are exposed by removing the mask (90).

As to claim 4, in Gruner's figure 2k, mask (91) is also considered as a follow-on mask, in Gruner's figure 2m mask (91) is removed from the top and sides.

As to claims 5, 6, Gruner's figure 2k, mask (91) replaces mask (90) and is aligned with the edges.

As to claim 7, masks (90) and (91) are sized to protect the critical edges.

As to claims 23-26, in the "Background Description" section on applicants' specification, applicants' disclose "As the size of semiconductor devices has decreased, photolithographic techniques become unable to reliably create structures of the dimensions required. As photolithographic techniques have become unusable, other technologies have been developed to create the small structures required by the ever shrinking semiconductor devices. One example of a non-photolithographic imaging technique is sidewall image transfer ("SIT")." [para 4]. It is noted that in the "Background Description" section on applicants' specification, applicants' are silent about the exact dimensions of what is considered as the "decreased" size, it would have been obvious to one of ordinary skill in the art at the time the invention was made to understand that sub-lithographic dimensions are typically in the range of few tens of nanometer since

the term few usually refers to 3-to-11, 11 tens of nanometers is 0.11 micrometers, which is in the sub-lithographic dimensions range.

Claim Rejections - 35 USC § 103

5. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gruner et al. (US 4,538,748) in view of Applicants' Admitted Prior Art, as applied to claims 1-8 above, and further in view of Nakai et al. (US 2005/0106837).

It is noted Gruner is silent about further comprising sizing the first portion of the follow-on mask to protect the critical edges of the hard mask when the follow-on mask is mis-registered by less than a predetermined amount.

Nakai teaches a method of manufacturing a semiconductor device citing "the alignment between the third window 111a and the fourth opening 105b is eased by making the size of the third window 111a of the second photoresist pattern 111 larger than that of the fourth opening 105b of the first hard mask 105." (paragraph 0130).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Gruner to size mask (90) to account for miss-alignment errors because Nakai teaches sizing a mask is conventionally performed for mask alignment purposes.

One of ordinary skill in the art would have been motivated to size a mask for mask alignment purposes in order to avoid properly expose (or cover) the desired structures edges when mask miss-alignment is a known and quantifiable issue.

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Response to Arguments

6. Applicant's arguments, filed 4/30/2008, with respect to the rejection(s) of all pending claims under 35 USC § 103 have been fully considered and are persuasive in view of the new amendments to the claims. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Applicants' Admitted Prior Art.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to MAHMOUD DAHIMENE whose telephone number is (571)272-2410. The examiner can normally be reached on week days from 8:00 AM. to 5:00 PM..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/M. D./ Examiner, Art Unit 1792

/Nadine G Norton/ Supervisory Patent Examiner, Art Unit 1792